## REMARKS

The Office Action of July 16, 2004 has been received and its contents carefully noted.

The present Amendment revises independent claim 1 to specify that a start signals is supplied to a CPU and to a second clock generating circuit substantially simultaneously. This is supported (for example) by the disclosure in dependent claim 2, which is being cancelled. The Amendment also revises claim 1 to recite that the start signal causes a clock generating circuit to start producing the second clock while the central processing unit is starting preparation for the interruption. This is supported (for example) by the disclosure in dependent claim 6, which is also being cancelled.

The present Amendment revises independent claim 17 along the lines discussed above with respect to claim 1. Dependent claim 18 is being cancelled.

In addition, the present Amendment revises independent claim 8 to recite that a CPU performs an interruption in accordance with a first clock. This is supported (for example) by the disclosure in dependent claim 14, which is being cancelled.

Finally, the present Amendment makes revisions in claims 1, 3, 4, and 7 that improvement agreement with antecedent recitations.

The Office Action rejects all of the claims for anticipation by U.S. patent 6,219,797 to Liu et al (which will hereafter be called simply "Liu"). For the reasons discussed below, however, it is respectfully submitted that the inventions now defined by the independent claims are patentable over this reference.

The Liu reference discloses a microprocessor which can operate with an external oscillator or, in a low power mode, with an internal oscillator. A passage noted in the

AMENDMENT 10/084,348

Office Action (at column 13 of the reference lines 31-36) explains that, in a "switchback" mode, operation can automatically return to a four clock per cycle speed when an interrupt occurs from an external source.

As was noted previously, claim 1 now provides that a start signal is supplied to both a CPU and to a second clock generating circuit substantially simultaneously, and that a clock generating circuit starts producing a second clock while the CPU is starting preparation for an interruption. Independent claim 17 is similar. These features are not disclosed in the Liu reference. Nor is there any apparent reason why an ordinarily skilled person who wanted to improve Liu's arrangement would have modified it so as to achieve what is now recited in claims 1 and 17.

Independent claim 8 recites "an interrupt control circuit for storing interruption data in accordance with the second clock ...", and also specifies that a CPU "performs the interruption in accordance with the first clock." Although Liu may change clock speeds during an interrupt, the reference neither discloses nor suggests using first and second clock signals in accordance with claim 8.

Finally, independent claim 19 recites "means for storing interruption data in accordance with the second clock" and "means for feeding the interruption data ... such that the central processing means performs the interruption with the interruption data in accordance with the first clock." As was the case with claim 8, this is neither disclosed nor suggested by the reference.

Since the remaining claims depend from the independent claims discussed above and recite additional limitations to further define the invention, they are patentable along with their independent claims and need not be further discussed.

AMENDMENT 10/084,348

For the foregoing reasons, it is respectfully submitted that this application is now in condition for allowance. Reconsideration of the application is therefore respectfully requested.

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Respectfully submitted,

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